Figure 1
Prior Art

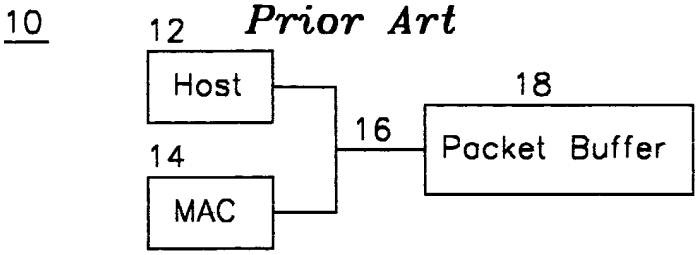


Figure 2

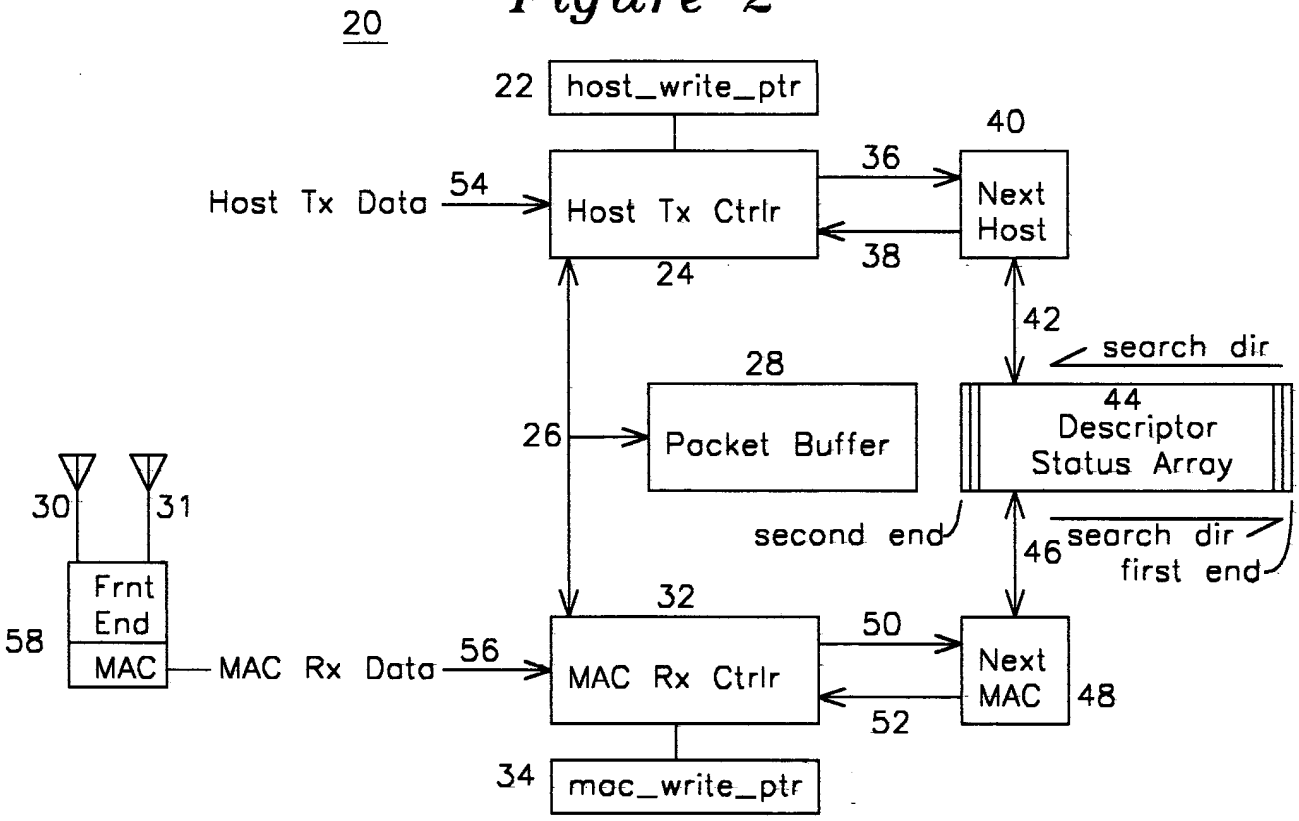


Figure 3

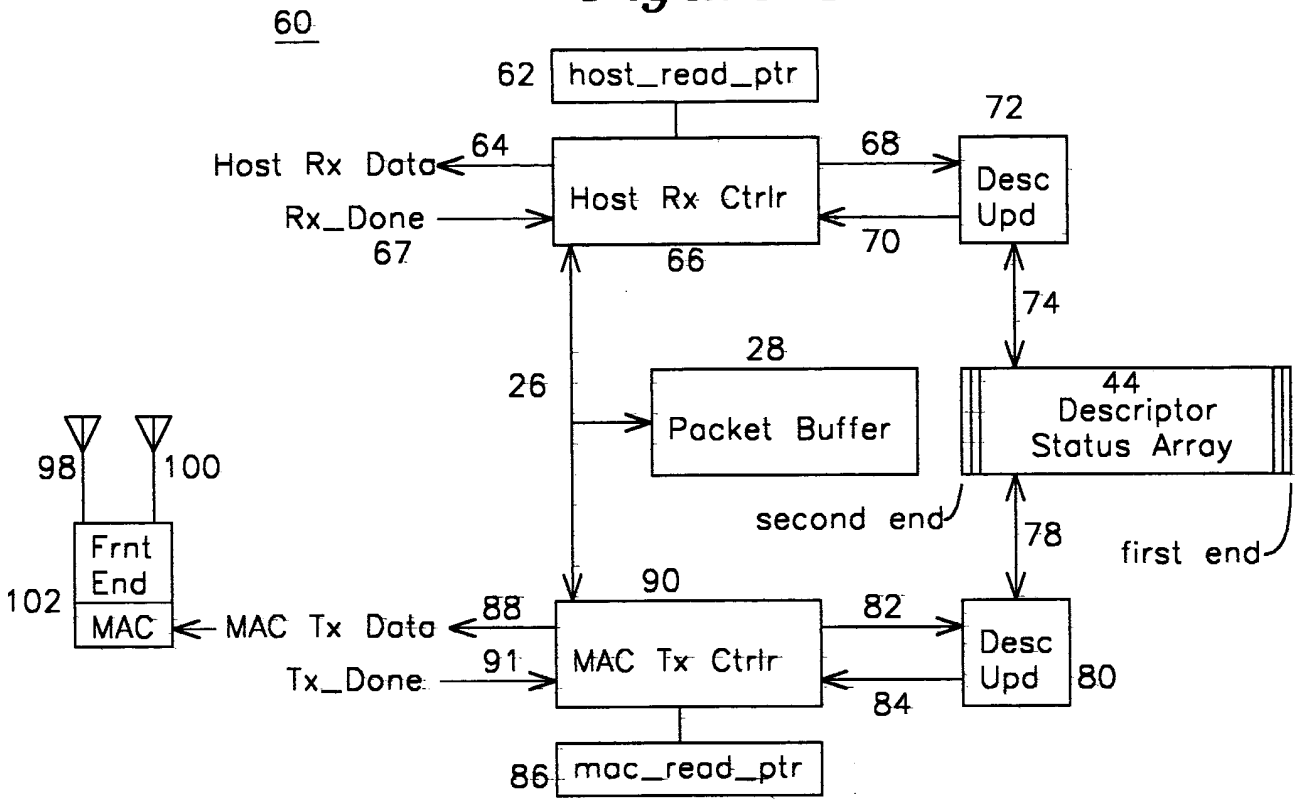


Figure 4

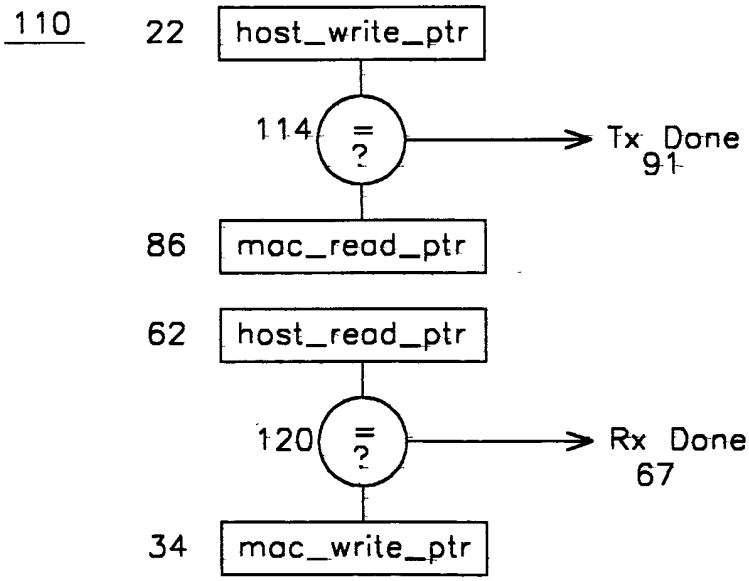


Figure 5

Single Queue Packet Memory

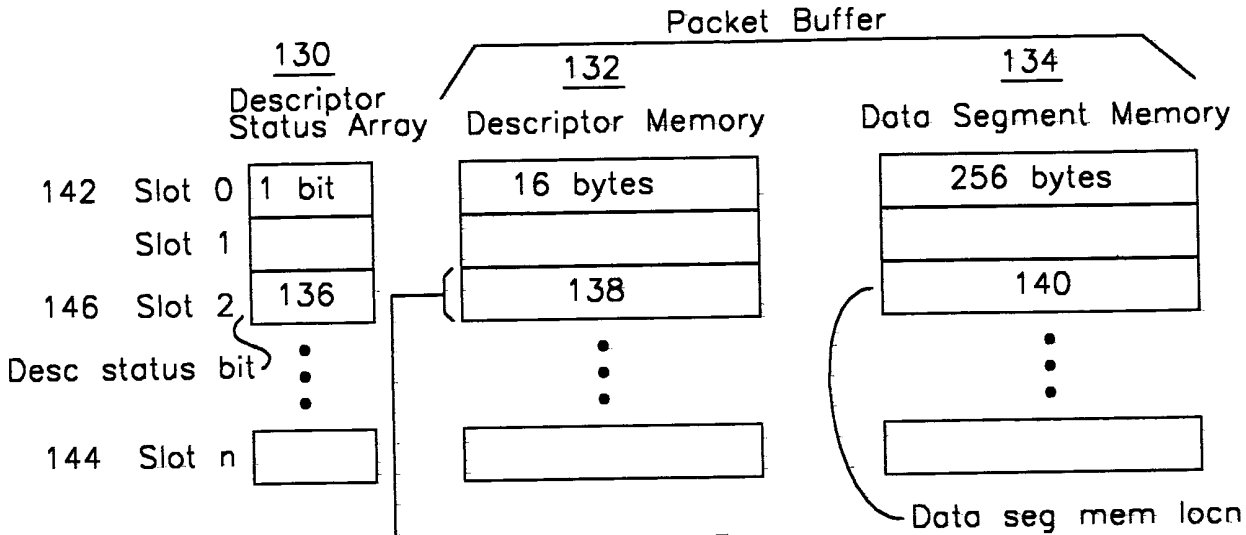


Figure 6

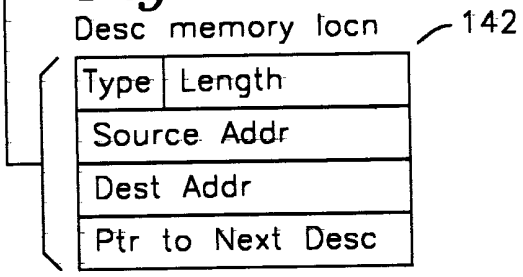


Figure 7

Multiple Queue Packet Memory

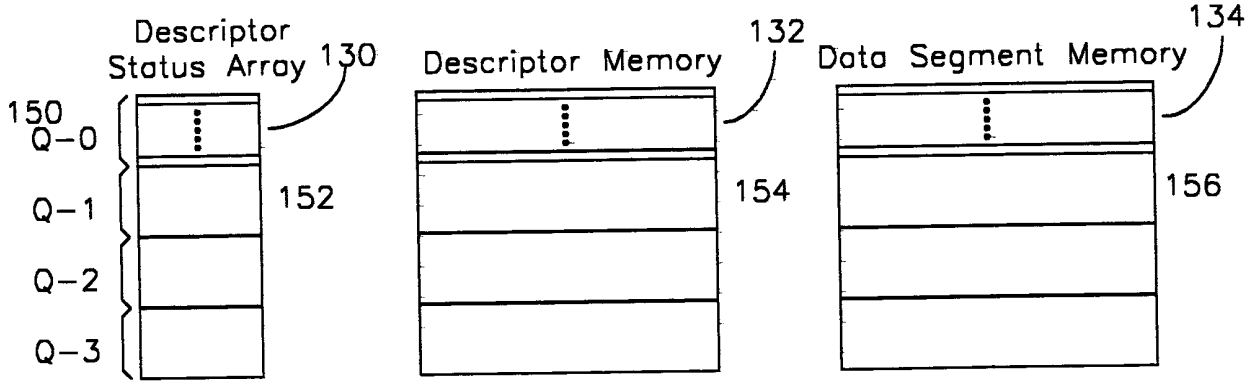


Figure 8a

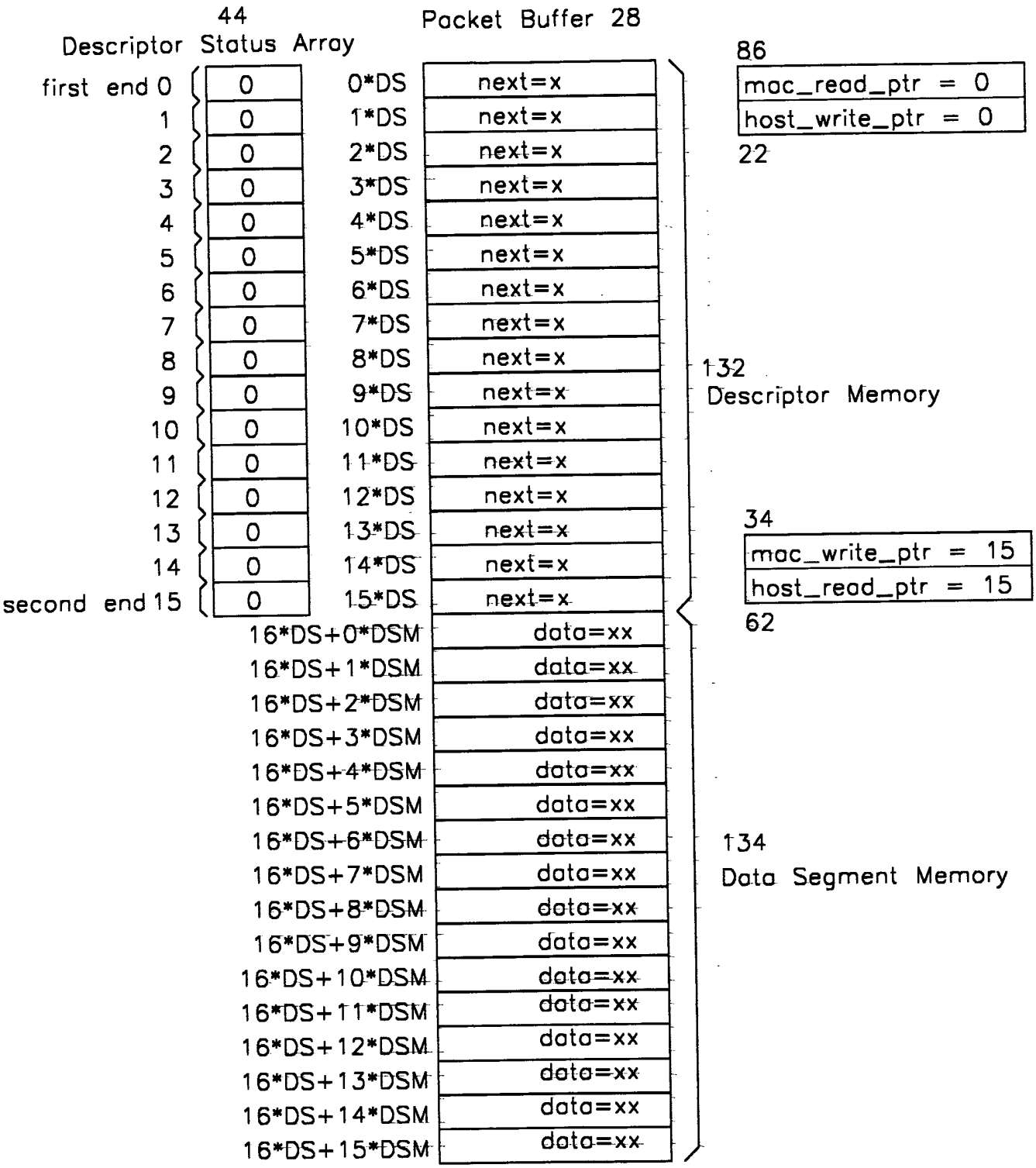

44
Descriptor Status Array
Packet Buffer 28
first end 0
second end 15
0*DS
1*DS
2*DS
3*DS
4*DS
5*DS
6*DS
7*DS
8*DS
9*DS
10*DS
11*DS
12*DS
13*DS
14*DS
15*DS
16*DS+0*DSM
16*DS+1*DSM
16*DS+2*DSM
16*DS+3*DSM
16*DS+4*DSM
16*DS+5*DSM
16*DS+6*DSM
16*DS+7*DSM
16*DS+8*DSM
16*DS+9*DSM
16*DS+10*DSM
16*DS+11*DSM
16*DS+12*DSM
16*DS+13*DSM
16*DS+14*DSM
16*DS+15*DSM
next=x
data=xx
86
mac_read_ptr = 0
host_write_ptr = 0
22
132
Descriptor Memory
34
mac_write_ptr = 15
host_read_ptr = 15
62
134
Data Segment Memory

Figure 8b

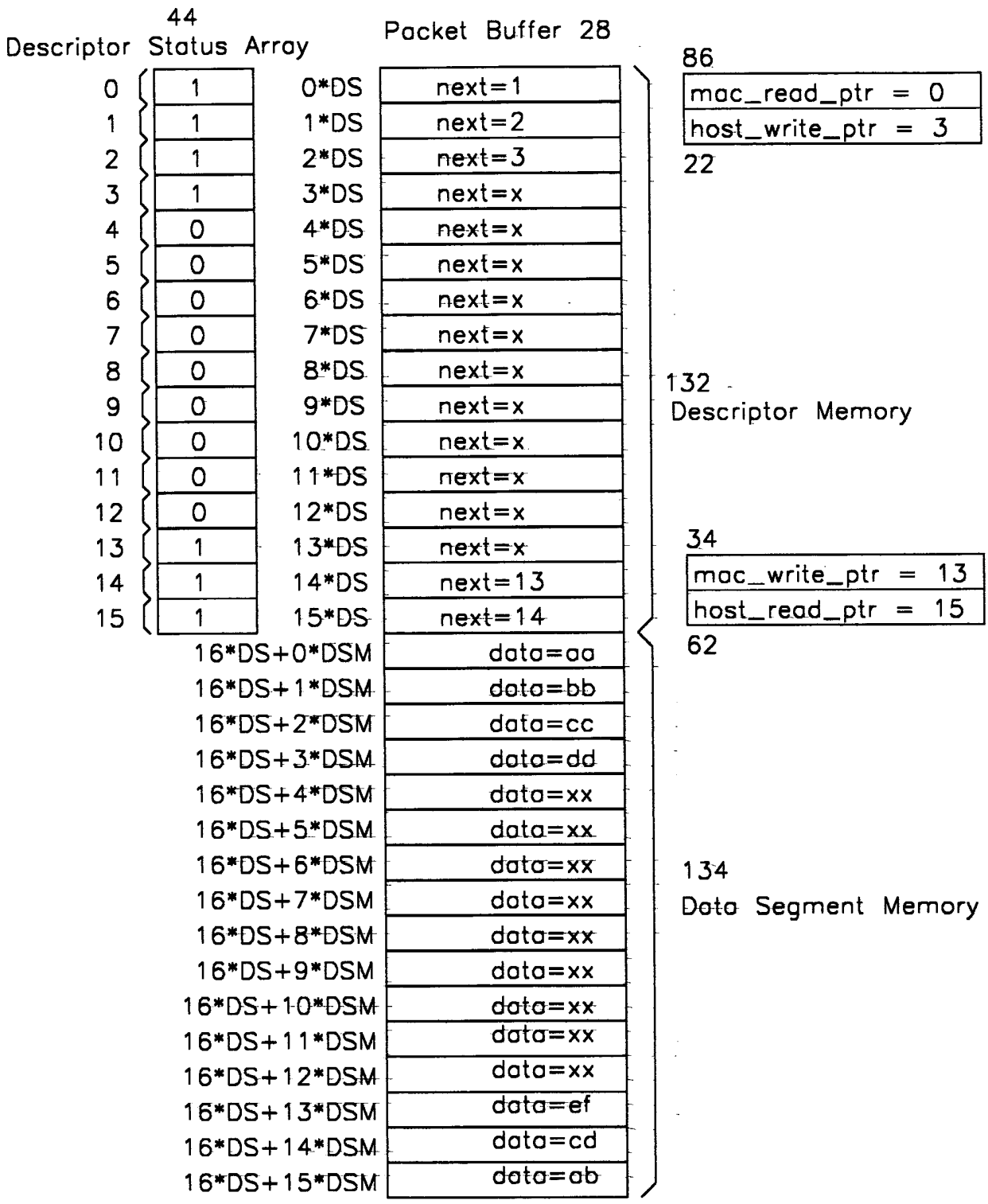

44
Descriptor Status Array
Packet Buffer 28
86
mac_read_ptr = 0
host_write_ptr = 3
22
0 1 0*DS next=1
1 1 1*DS next=2
2 1 2*DS next=3
3 1 3*DS next=x
4 0 4*DS next=x
5 0 5*DS next=x
6 0 6*DS next=x
7 0 7*DS next=x
8 0 8*DS next=x
9 0 9*DS next=x
10 0 10*DS next=x
11 0 11*DS next=x
12 0 12*DS next=x
13 1 13*DS next=x
14 1 14*DS next=13
15 1 15*DS next=14
132
Descriptor Memory
34
mac_write_ptr = 13
host_read_ptr = 15
62
16*DS+0*DSM data=aa
16*DS+1*DSM data=bb
16*DS+2*DSM data=cc
16*DS+3*DSM data=dd
16*DS+4*DSM data=xx
16*DS+5*DSM data=xx
16*DS+6*DSM data=xx
16*DS+7*DSM data=xx
16*DS+8*DSM data=xx
16*DS+9*DSM data=xx
16*DS+10*DSM data=xx
16*DS+11*DSM data=xx
16*DS+12*DSM data=xx
16*DS+13*DSM data=ef
16*DS+14*DSM data=cd
16*DS+15*DSM data=ab
134
Data Segment Memory

Figure 8c

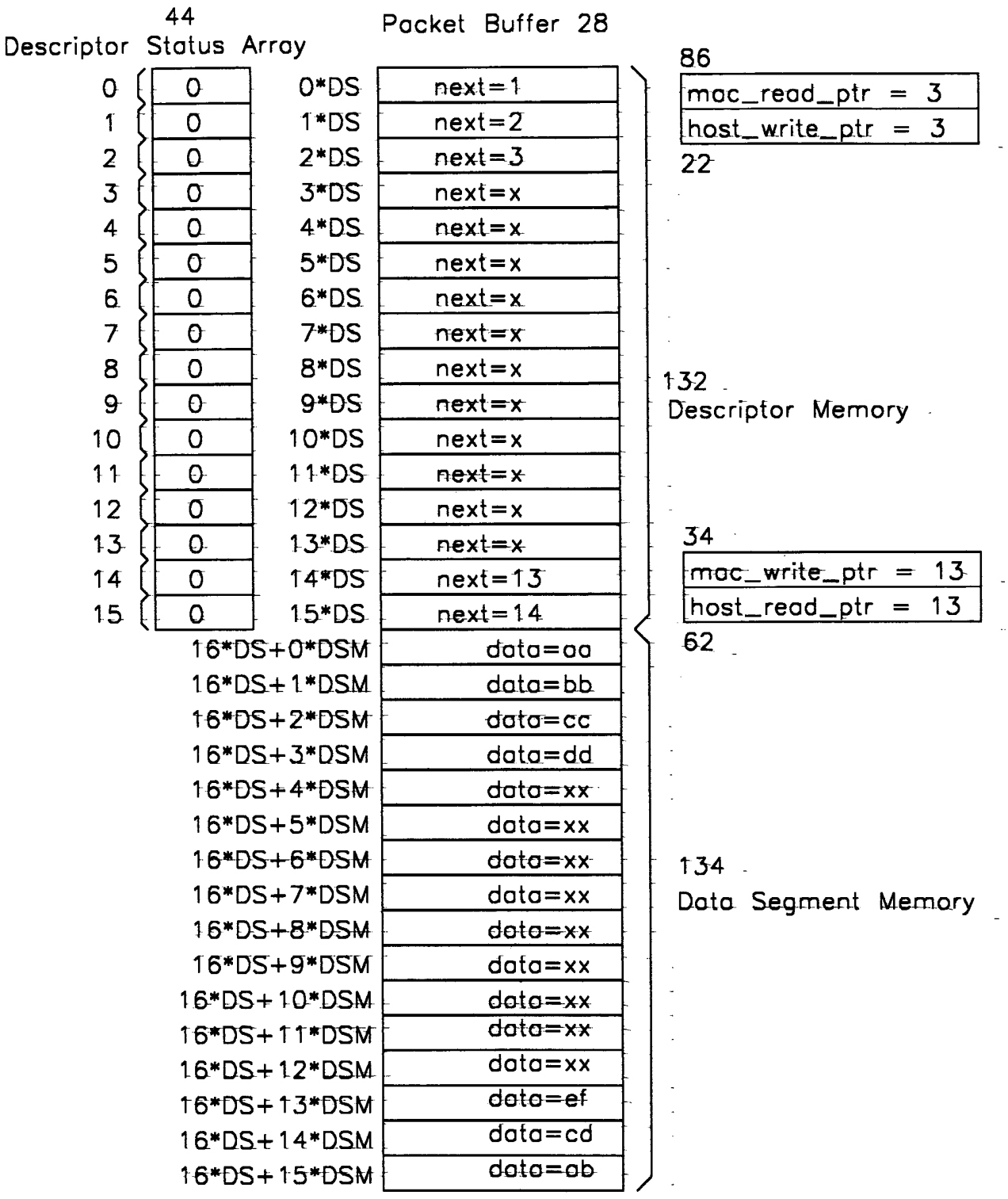

44
Descriptor Status Array
Packet Buffer 28
0 0 0*DS next=1
1 0 1*DS next=2
2 0 2*DS next=3
3 0 3*DS next=x
4 0 4*DS next=x
5 0 5*DS next=x
6 0 6*DS next=x
7 0 7*DS next=x
8 0 8*DS next=x
9 0 9*DS next=x
10 0 10*DS next=x
11 0 11*DS next=x
12 0 12*DS next=x
13 0 13*DS next=x
14 0 14*DS next=13
15 0 15*DS next=14
16*DS+0*DSM data=aa
16*DS+1*DSM data=bb
16*DS+2*DSM data=cc
16*DS+3*DSM data=dd
16*DS+4*DSM data=xx
16*DS+5*DSM data=xx
16*DS+6*DSM data=xx
16*DS+7*DSM data=xx
16*DS+8*DSM data=xx
16*DS+9*DSM data=xx
16*DS+10*DSM data=xx
16*DS+11*DSM data=xx
16*DS+12*DSM data=xx
16*DS+13*DSM data=ef
16*DS+14*DSM data=cd
16*DS+15*DSM data=ab
86
mac_read_ptr = 3
host_write_ptr = 3
22
132
Descriptor Memory
34
mac_write_ptr = 13
host_read_ptr = 13
62
134
Data Segment Memory

Figure 9

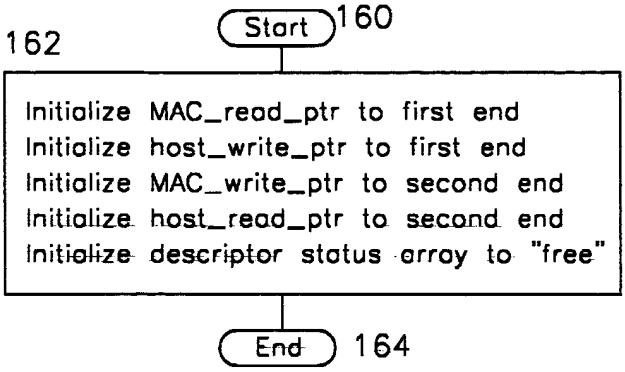


Figure 10a

Host Tx Controller Process

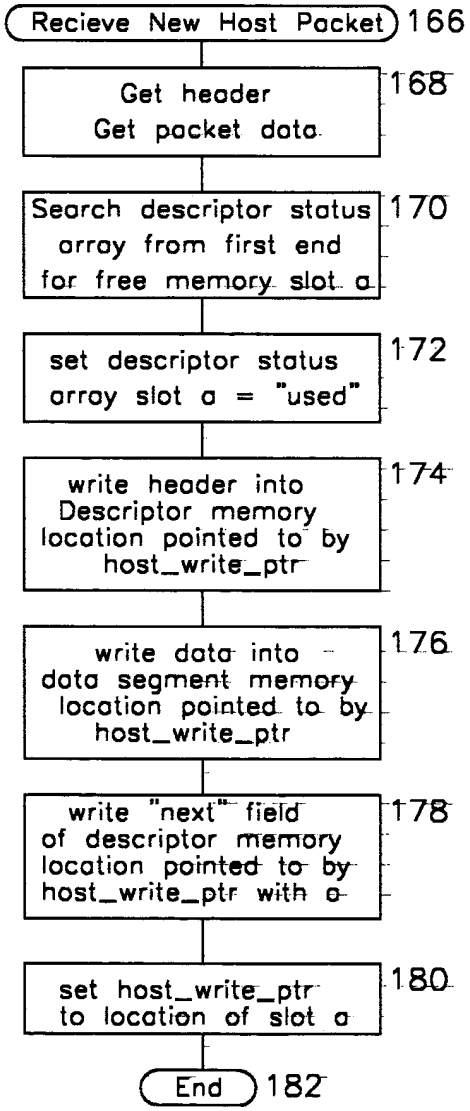

Recieve New Host Packet
166
Get header
Get packet data
168
Search descriptor status array from first end for free memory slot a
170
set descriptor status array slot a = "used"
172
write header into Descriptor memory location pointed to by host_write_ptr
174
write data into data segment memory location pointed to by host_write_ptr
176
write "next" field of descriptor memory location pointed to by host_write_ptr with a
178
set host_write_ptr to location of slot a
180
End
182

Figure 10b

MAC Rx Controller Process

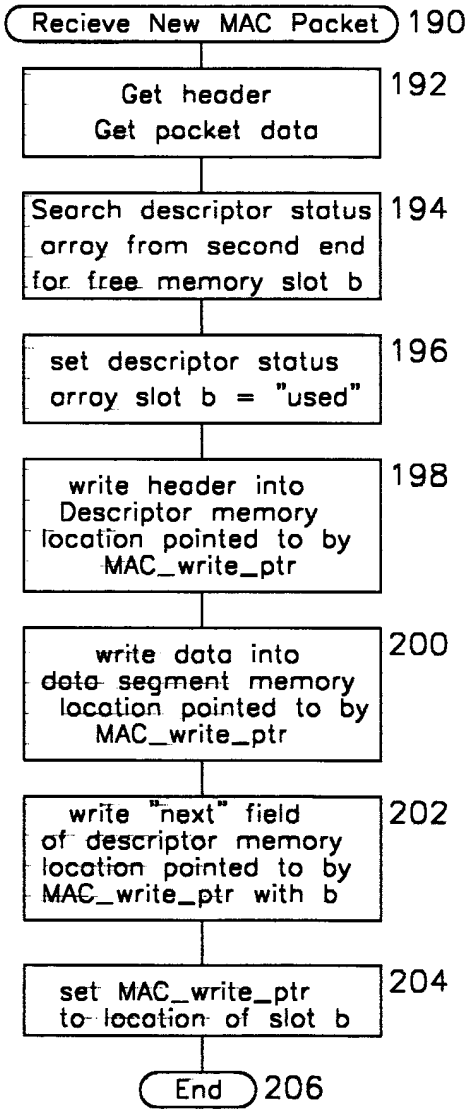

Recieve New MAC Packet
190
Get header
Get packet data
192
Search descriptor status array from second end for free memory slot b
194
set descriptor status array slot b = "used"
196
write header into Descriptor memory location pointed to by MAC_write_ptr
198
write data into data segment memory location pointed to by MAC_write_ptr
200
write "next" field of descriptor memory location pointed to by MAC_write_ptr with b
202
set MAC_write_ptr to location of slot b
204
End
206

Figure 11a

Host Rx Controller Process

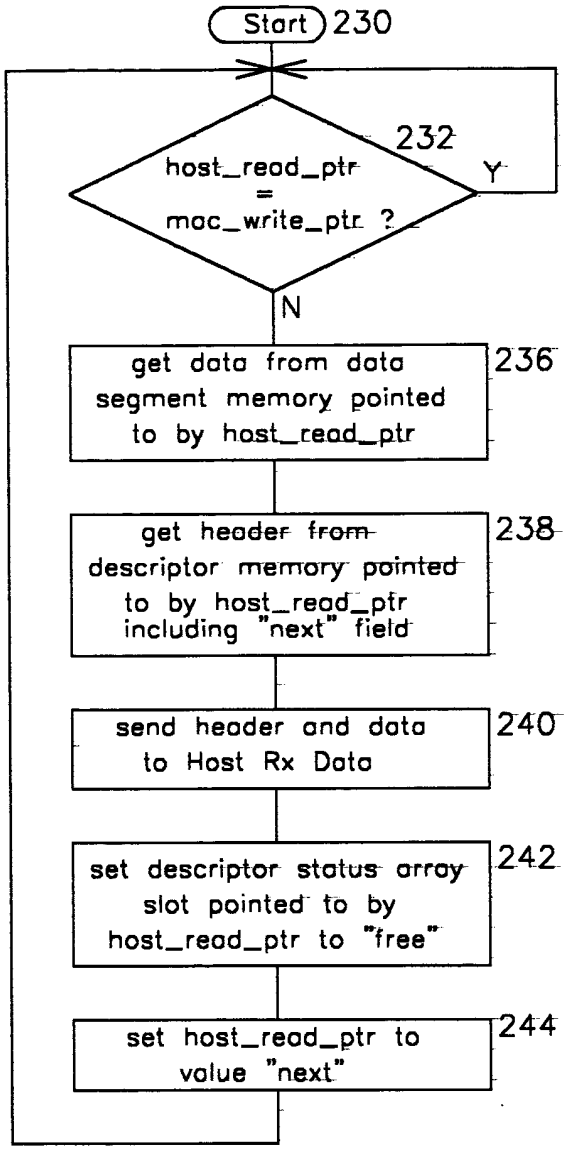
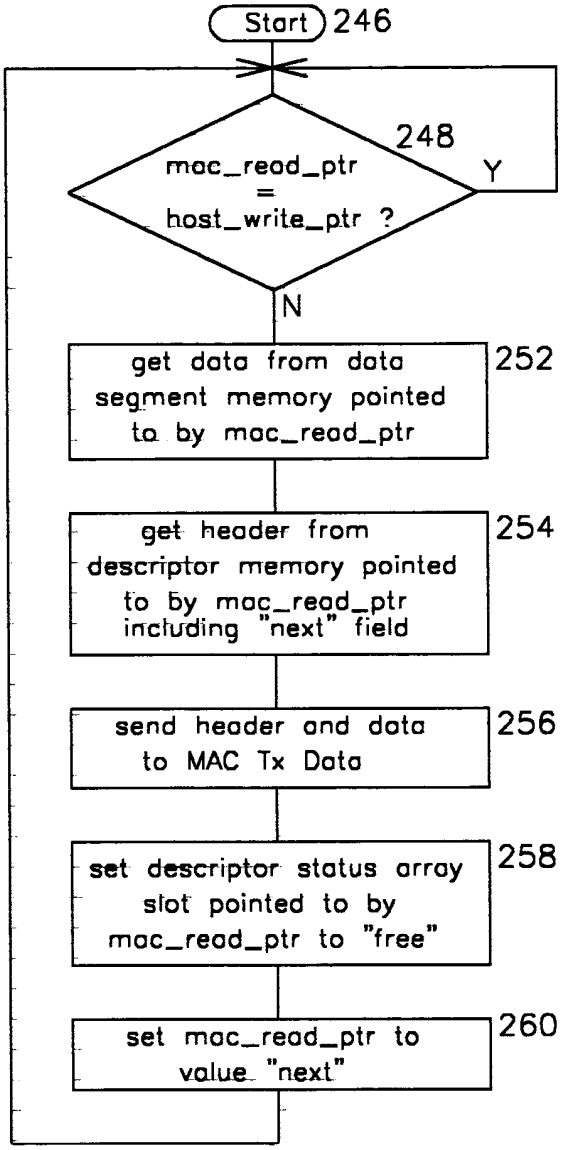


Figure 11b

MAC Tx Controller Process